	Application No.	Applicant(s)
	10/796,156	WENG, RUEY-SHING
Notice of Allowability	Examiner	Art Unit
	Kevin M. Nguyen	2629
The MAILING DATE of this communication app All claims being allowable, PROSECUTION ON THE MERITS IS herewith (or previously mailed), a Notice of Allowance (PTOL-85 NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT R of the Office or upon petition by the applicant. See 37 CFR 1.31	ears on the cover sheet with t	n this application. If not included unication will be mailed in due course. THIS
1. \square This communication is responsive to $\underline{3/10/2004}$.		
2. The allowed claim(s) is/are <u>1-14</u> .		
 Acknowledgment is made of a claim for foreign priority under a) All b) Some* c) None of the: Certified copies of the priority documents have Certified copies of the priority documents have Copies of the certified copies of the priority documents have International Bureau (PCT Rule 17.2(a)). 	e been received. e been received in Applicatio	on No
* Certified copies not received:		
Applicant has THREE MONTHS FROM THE "MAILING DATE" noted below. Failure to timely comply will result in ABANDON! THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.	MENT of this application.	
4. A SUBSTITUTE OATH OR DECLARATION must be subm INFORMAL PATENT APPLICATION (PTO-152) which giv		
5. CORRECTED DRAWINGS (as "replacement sheets") mu	st be submitted.	
(a) ☐ including changes required by the Notice of Draftsper	son's Patent Drawing Review	v (PTO-948) attached
1) 🗌 hereto or 2) 🔲 to Paper No./Mail Date	_•	
(b) ☐ including changes required by the attached Examiner Paper No./Mail Date Identifying indicia such as the application number (see 37 CFR)		
each sheet. Replacement sheet(s) should be labeled as such in	the header according to 37 CF	FR 1.121(d).
 DEPOSIT OF and/or INFORMATION about the deposit attached Examiner's comment regarding REQUIREMENT 		
Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)		formal Patent Application ummary (PTO-413),
	Paper No./	/Mail Date . /
 3. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 3/10/04 4. Examiner's Comment Regarding Requirement for Deposit of Biological Material 		Amendment/Comment Statement of Reasons of Allowance RICHARD NUEHPE SUPERVISORY PATENT EXAMINER TECHNIOLOGY CENTER 2000

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REASONS FOR ALLOWANCE

- 1. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oomura (US 6,693,388) discloses an active matrix display is provided which eliminates variation of a threshold voltage of an active element inside a pixel (see the abstract). Kawasaki et al (US 6,909,410) discloses a driving circuit for a light-emitting element in which it is possible to exactly control a current flown in the light emitting element, and perform a stable operation while reducing a power-supply voltage as low as possible (see the abstract). Okabe et al (US 2003/0112208) discloses a selfluminous display which prevents, in a driving circuit of a spontaneous light emitting type display device using an active matrix method, a noise current from flowing in a light emitting element when compensating for a threshold voltage of a transistor for controlling current flowing to the emitting element to thereby enhance precision in a luminance (see the abstract). Lo (US 2005/0068274) discloses driving apparatus and method for active matrix organic light emitting display which employs an auto-zero mechanism to compensate threshold voltage variations of each driving element to improve image uniformity (see the abstract).
- 2. Claims 1-14 are allowed.
- 3. The following is an examiner's statement of reasons for allowance:

Independent claim 1 is allowable because the cited prior art, single or combination, does not teach or suggest "[a]n active matrix display driving circuit is disclosed and a driving circuit of each pixel on a display panel includes: a first scan

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transistor and a second scan transistor, the gates (G) of the first scan transistor and second scan transistor connected to a scan line and sources (S) connected to a data line; a driving transistor, the source (S) of the driving transistor connected to a voltage supply; a connect transistor, the source (S) of the connect transistor connected to drains (D) of driving transistor and second scan transistor and gate (G) connected to an emission line; a first switch transistor, the source (S) of the first switch transistor connected to a first voltage supply and gate (G) connected to a scan line; a second switch transistor, the source (S) of the second switch transistor connected to a second voltage supply and gate (G) connected to the emission line; a storage capacitor, one end of the storage capacitor connected to drains (D) of the first switch transistor and second switch transistor and the other end connected to drain (D) of the first scan transistor and gate (G) of the driving transistor; a luminescence device, the anode of the luminescence device connected to drain (D) of the connect transistor and the cathode connected to the ground."

Independent claim 8 is allowable because the cited prior art, single or combination, does not teach or suggest "[a]n active matrix display driving circuit is disclosed and a driving circuit of each pixel on a display panel includes one scan line and one data line as follows: a first scan transistor and a second scan transistor, the gates (G) of the first scan transistor and second scan transistor connected to a scan line and sources (S) connected to a data line; a driving transistor, the source (S) of the driving transistor grounded; a connect transistor, the source (S) of the connect transistor connected to drains (D) of driving transistor and first scan transistor and gate (G)

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connected to an emission line; a first switch transistor, the source (S) of the first switch transistor connected to a first voltage supply and gate (G) connected to a scan line; a second switch transistor, the source (S) of the second switch transistor connected to a second voltage supply and gate (G) connected to the emission line; a storage capacitor, one end of the storage capacitor connected to drains (D) of the first switch transistor and second switch transistor and the other end connected to drain (D) of the second scan transistor and gate (G) of the driving transistor; a luminescence device, the anode of the luminescence device connected to voltage supply and cathode connected to drain (D) of the connect transistor."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to KEVIN M. NGUYEN whose telephone number is 571-272-7697. The examiner can normally be reached on MON-THU from 8:00-6:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, a supervisor RICHARD A. HJERPE can be reached on 571-272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8000.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the Patent Application Information Retrieval system, see http://portal.uspto.gov/external/portal/pair. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Nguyen Patent Examiner Art Unit 2629

KMN September 19, 2006

> RICHARD HJERPE SUPERVISORY PATENT EXAMINER TECHNOLOGY CENTER 2600